ABSTRACT OF THE DISCLOSURE

In a semiconductor memory device comprising a cell array of memory cells each including a cell transistor and a capacitor, word lines and bit line pairs, the control circuit controls the memory circuit to set the bit lines to a high level to write "1" data into the memory cells regardless of a logic level of data to be written, in a state where a potential of a gate of the cell transistor of each memory cell is raised from a first potential of a standby time to a second potential of an active time, and thereafter to set the bit lines to a low level to write "0" data into the memory cells with "0" data to be written, in a state where the potential of the gate of the cell transistor is changed to a third potential higher than the first potential and lower than the second potential.